Integrated Circuits in 1958
The first single-chip microprocessor, circa 1971

(Intel 4004: 740kHz, 4-bit, 4KB cache, 2,300 transistors)
microprocessors, circa 2011

(Intel Gulftown 6-core processor - 1.17B transistors)
The M microcontroller
The M2 microcontroller
28-pin DIP
8-bit Atmel ATmega32U4 processor
16 MHz clock
25 I/O pins
12 channel 10-bit ADC
32k Flash, 1k EEPROM, 2.5k SRAM
4 independent timers with PWM
USART, I2C, SPI, JTAG, USB
The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega16U4/ATmega32U4 provides the following features: 16/32K bytes of In-System Programable Flash with Read-While-Write capabilities, 512Bytes/1K bytes EEPROM, 1.25/2.5K bytes SRAM, 26 general purpose I/O lines (CMOS outputs and LVTTL inputs), 32 general purpose working registers, four flexible Timer/Counters with compare modes and PWM, one more high-speed Timer/Counter with compare modes and PLL adjustable source, one USART (including CTS/RTS flow control signals), a byte oriented 2-wire Serial Interface, a 12-
take a break
and go learn
binary
Microcontroller Architectures

A Von Neumann architecture computer uses a shared pathway for instructions and data to/from the CPU.

A Harvard architecture computer uses separate pathways for instructions and data.
Memory Map

32k Flash
"Program Memory"

CPU

2.5k SRAM
"Data Memory"

Instruction (16 or 32 bit)
Address (16 bit)

Data (8 bit)
Address (16 bit)
Memory Map

2.5k SRAM
"Data Memory"

address: 0x02A5
value: 0x2F

MSB MSB
0 0 1 0 1 1 1 1

LSB

working reg
I/O
ext. I/O
SRAM

0x0000 0x0020 0x0060 0x0100 0x0100 0x0AFF