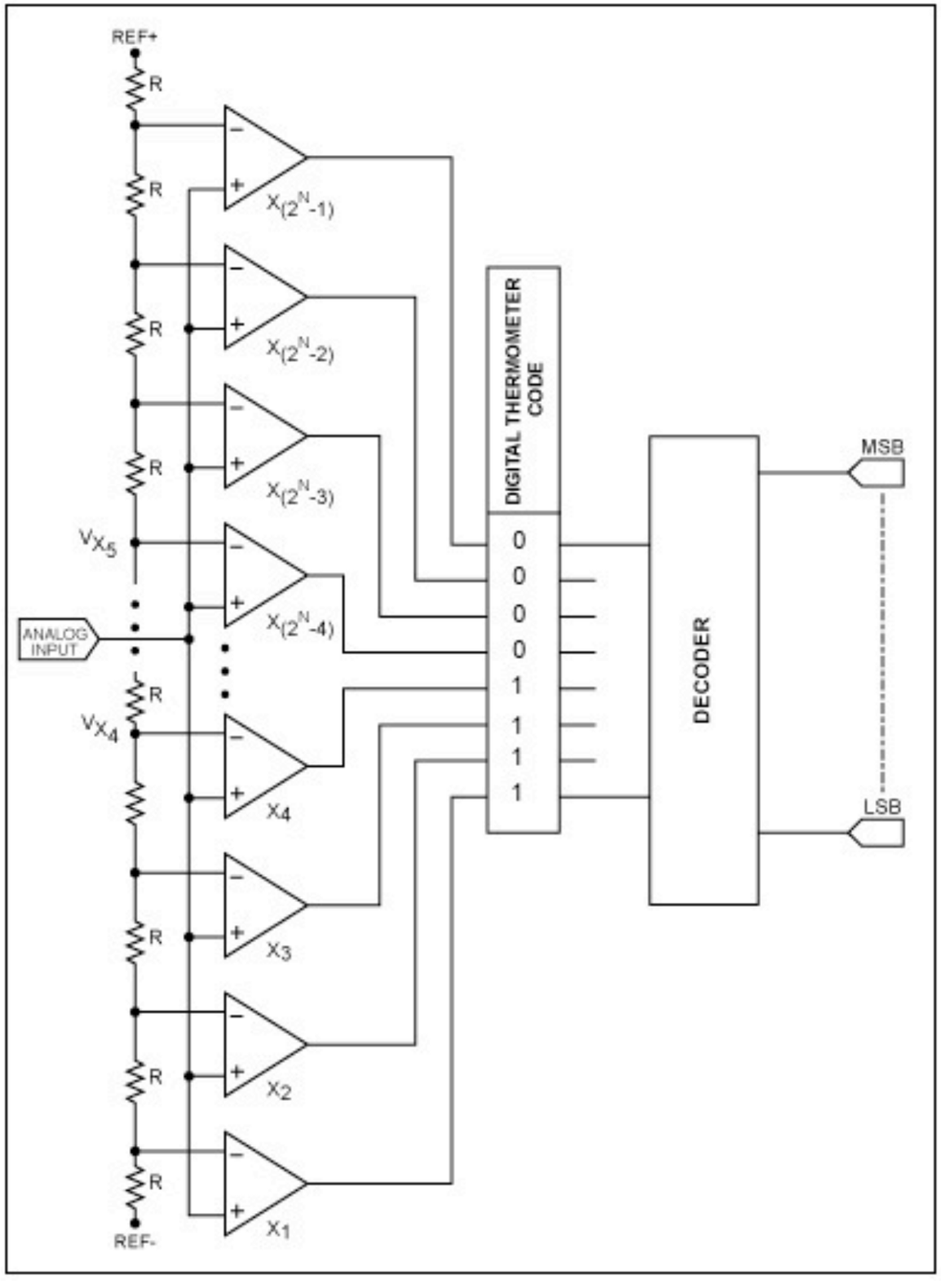
Analog-to-Digital Conversion

http://joeyroth.com/ceramic-speakers/

Common ADC Architectures

Flash

- cascade of n comparators
- fastest (Gsps)
- low resolution (n ~ 8)
- more expensive



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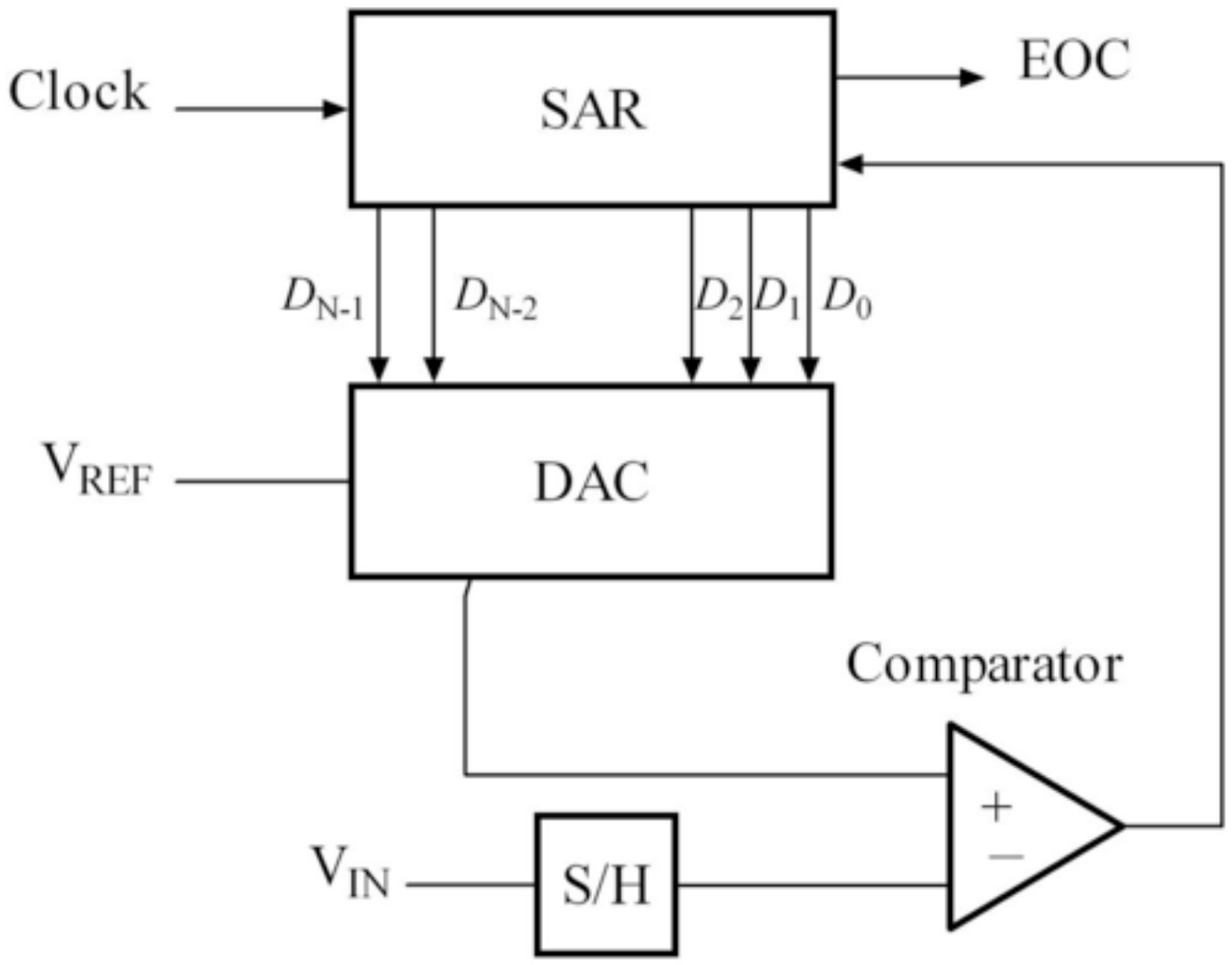
Successive Approximation

- compares input to internal DAC
- starts with MSB
- successively updates DAC to match
- mid-range speed (Msps)



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Sigma-Delta

- oversamples then filters
- highest possible resolution
- lower-speed (<Msps)

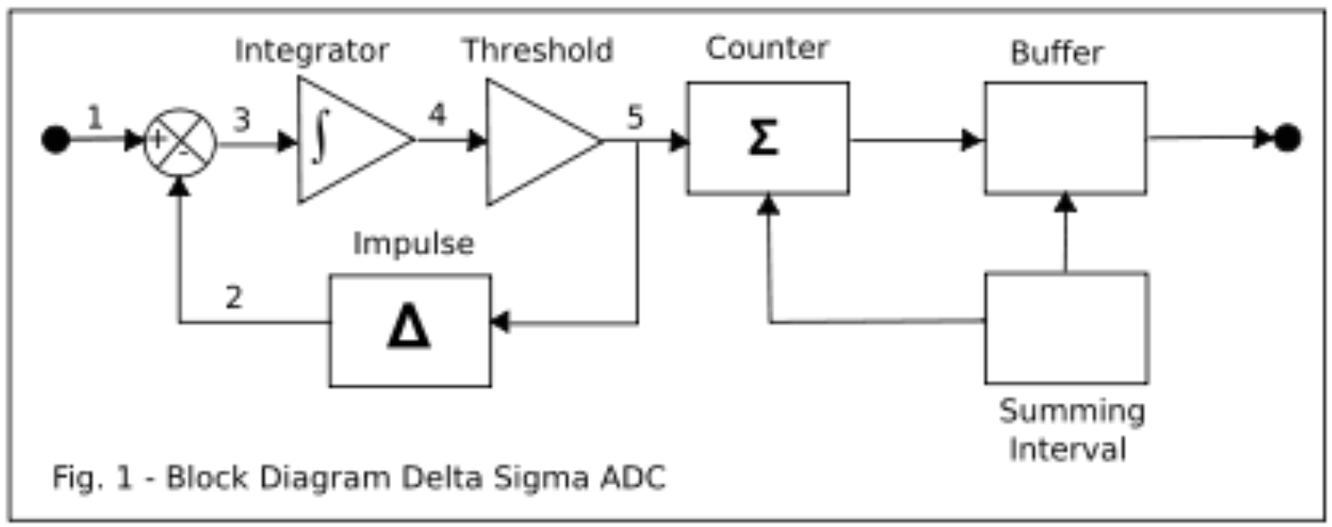

Fig. 1 - Block Diagram Delta Sigma ADC

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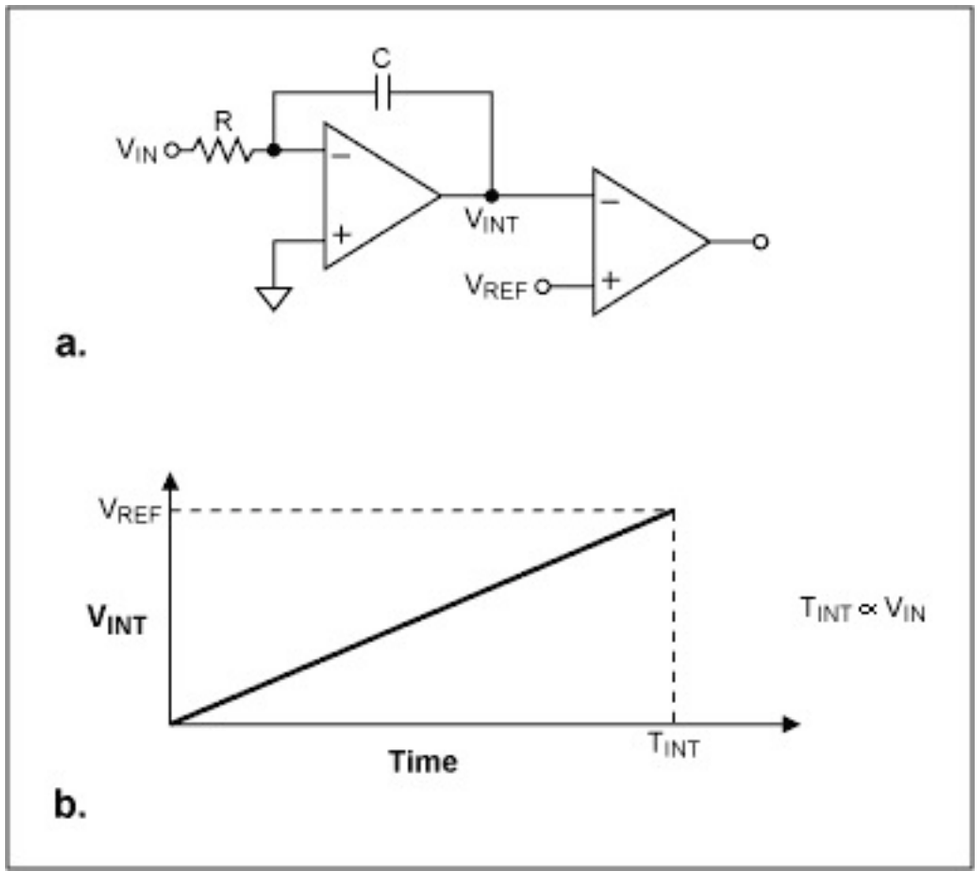
Integrating

- compares against ramp reference
- counts time until compare
- lowest-speed (<100ksps)



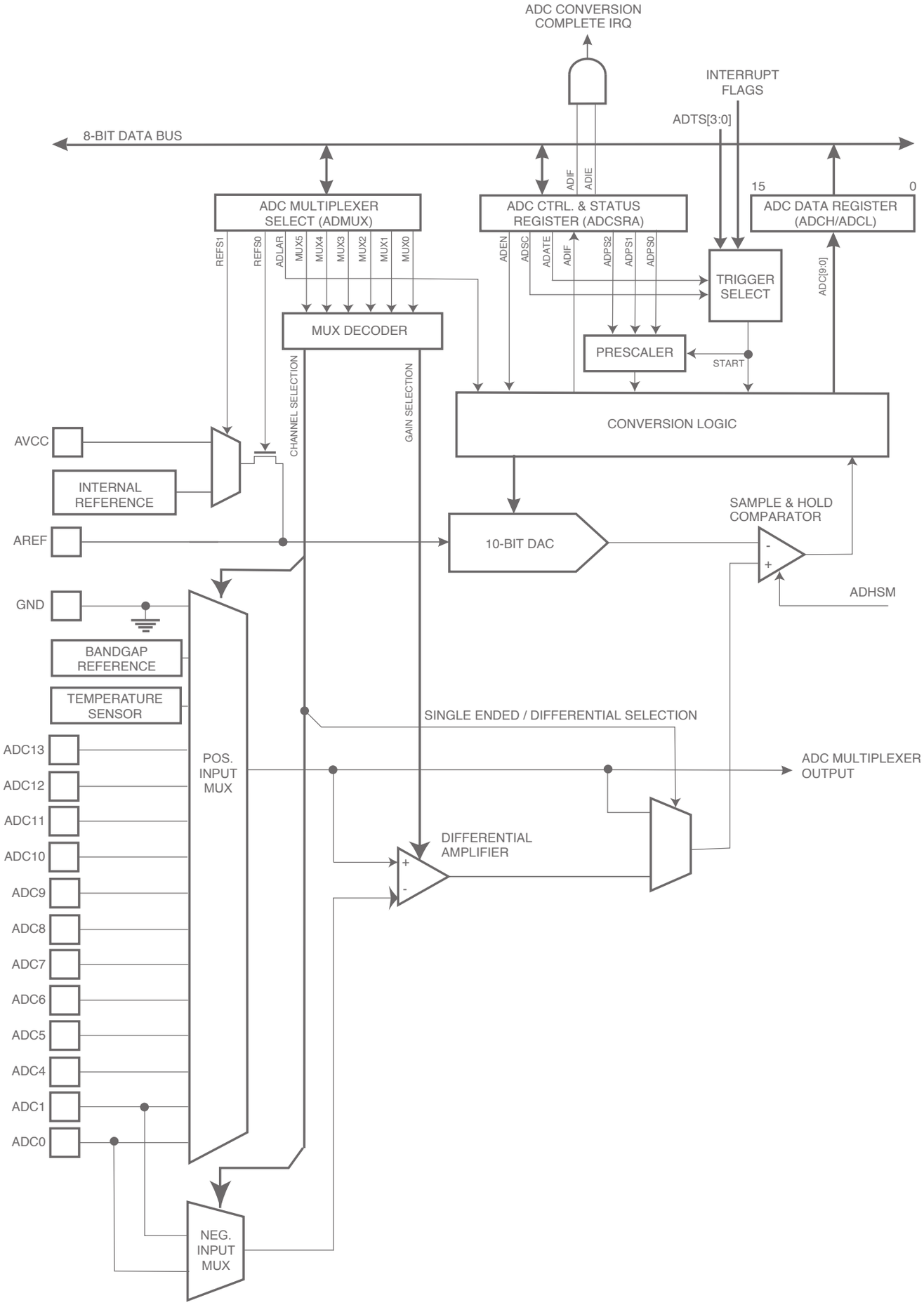
ATmega32U4 ADC

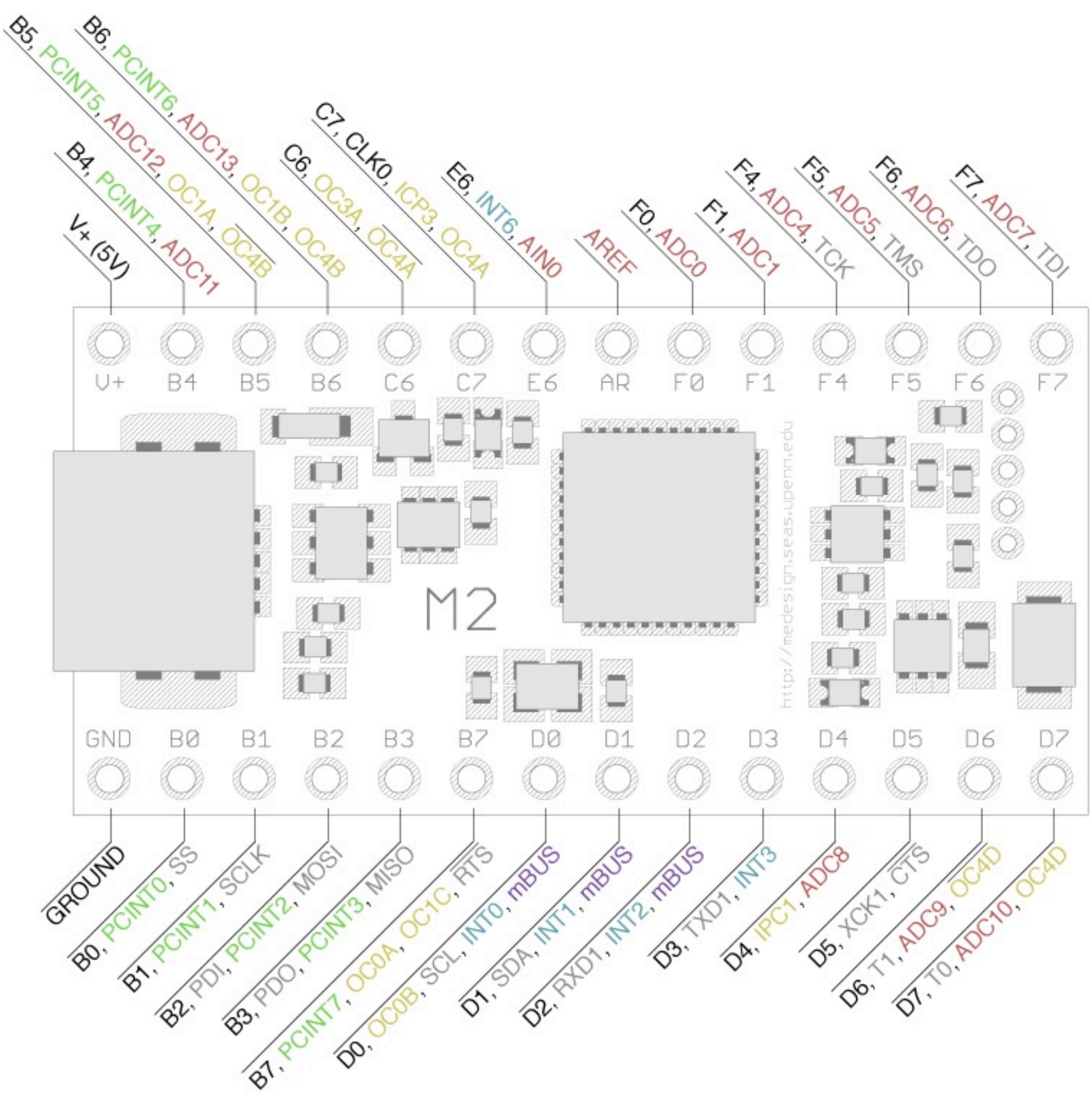
10-bit

successive approximation

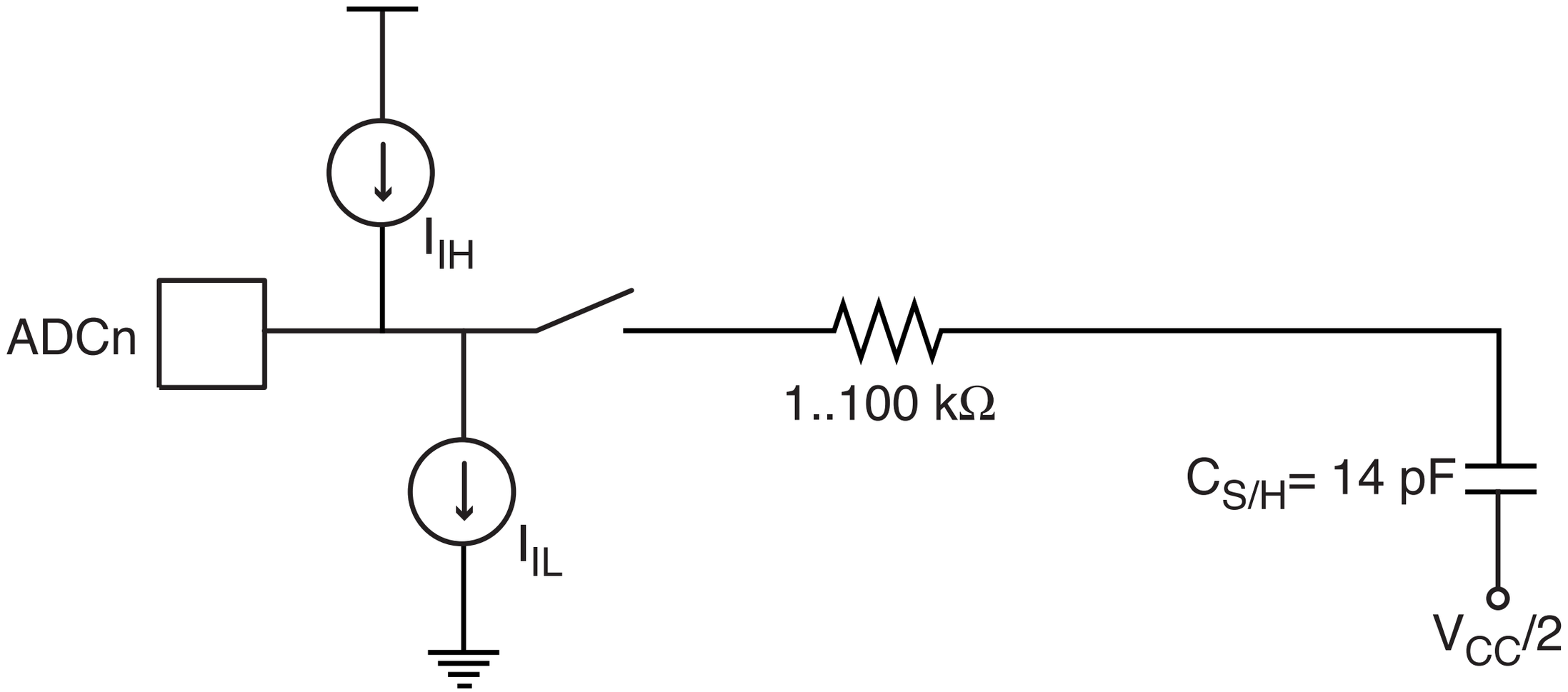
12 channels

up to 15 ksps

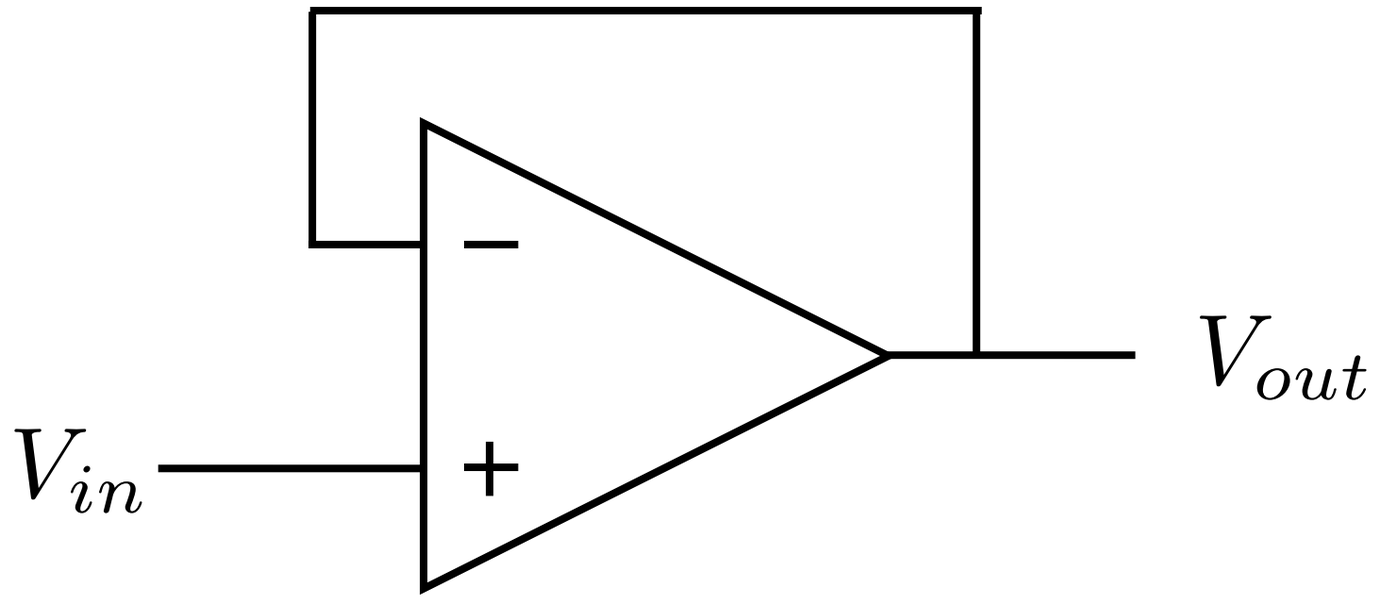



B5, PCINT5, ADC12, OC1A, OC4B
B6, PCINT6, ADC13, OC1B, OC4B
C7, CLK0, ICP3, OC4A
C6, OC3A, OC4A
E6, INT6, AIN0
AREF
F0, ADC0
F1, ADC1
F4, ADC4, TCK
F5, ADC5, TMS
F6, ADC6, TDO
F7, ADC7, TDI
V+ (5V)
B4, PCINT4, ADC11
V+ B4 B5 B6 C6 C7 E6 AR F0 F1 F4 F5 F6 F7
M2
http://medesign.seas.upenn.edu
GND B0 B1 B2 B3 B7 D0 D1 D2 D3 D4 D5 D6 D7
GROUND
B0, PCINT0, SS
B1, PCINT1, SCLK
B2, PDI, PCINT2, MOSI
B3, PDO, PCINT3, MISO
B7, PCINT7, OC0A, OC1C, RTS
D0, OC0B, SCL, INT0, mBUS
D1, SDA, INT1, mBUS
D2, RXD1, INT2, mBUS
D3, TXD1, INT3
D4, IPC1, ADC8
D5, XCK1, CTS
D6, T1, ADC9, OC4D
D7, T0, ADC10, OC4D

ADC : inputs



ADC : inputs - buffering!



$$V_{out} = V_{in}$$

high-impedance input
low-impedance output

ADC : inputs

Anti-Aliasing & The Nyquist Theorem

$$N > 2f_{max}$$

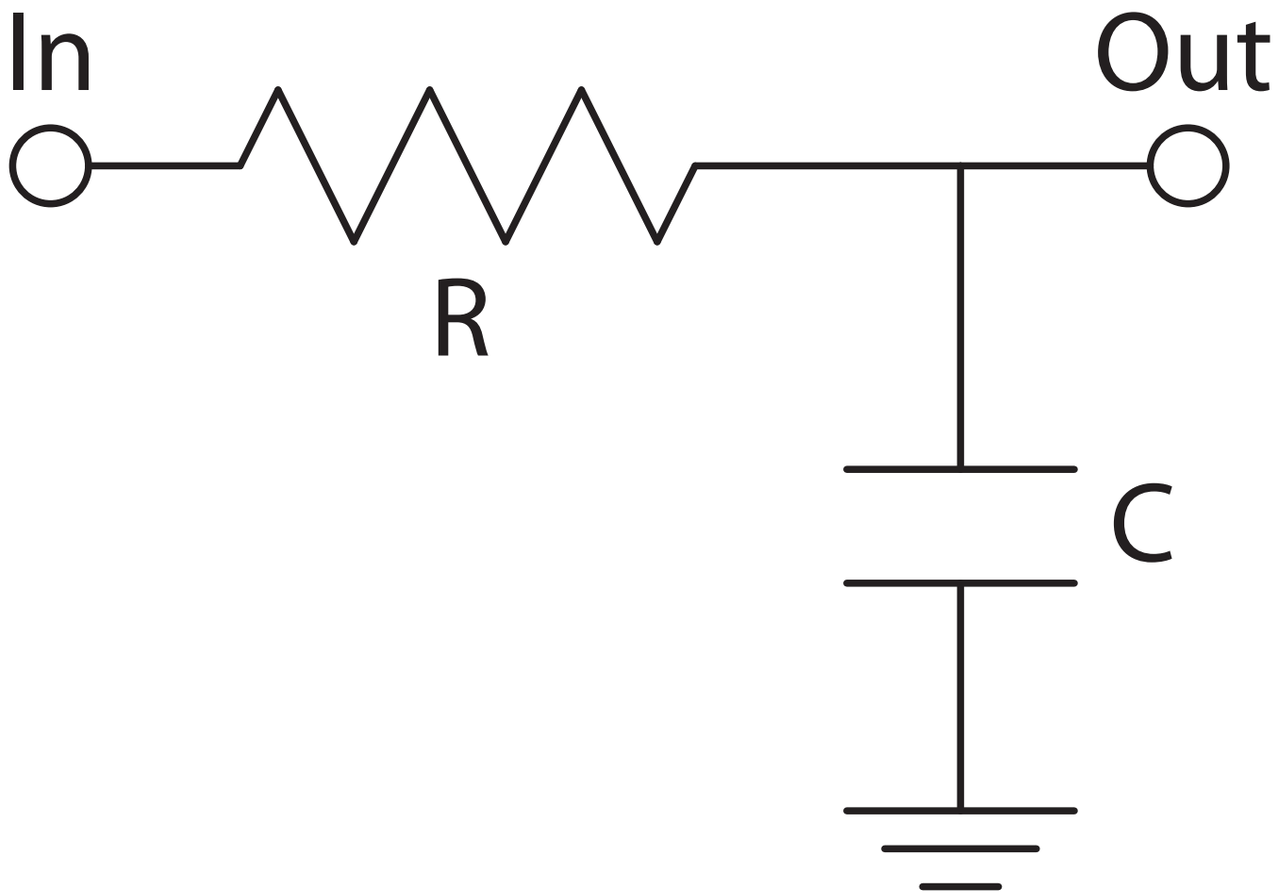
sampling rate

maximum desired frequency

Add a buffered RC low-pass filter before the input to the microcontroller

recommended cutoff < 100 kHz

ADC : inputs - filtering!



$$f_c = \frac{1}{2\pi RC}$$

ADC : process

set the voltage reference

set the ADC clock prescaler

disable some digital inputs

set up interrupts and triggering, if desired

select the desired analog input

enable conversions

start the conversion process

read the result

ADC : voltage reference

setting the MAX value (0x03FF) to one of the following:

external AREF (default!)

Vcc

2.56V

ADMUX : REFS1, REFS0

ADC : prescaler

set ADC clock to 50-200kHz

driven from system clock

ADCSRA : ADPS2, ADPS1, ADPS0

ADC : digital disable

turn off the digital input circuitry

DIDR0 : ADCnD (for n=0...7)
DIDR2 : ADCnD (for n=8...13)

ADC : triggering

single-conversion (leave alone)

vs.

free-running

ADCSRA : ADATE

ADC : input selection

single ADC unit

12 multiplexed inputs

ADCSRA : MUX5
ADMUX : MUX2, MUX1, MUX0

ADC: enable and start

must enable and start conversion

ADCSRA :ADEN
ADCSRA :ADSC

ADC: results

16-bit pseudoregister